MKR

Notice of Allowability	Application No.	Applicant(s)	
	10/698,136	KEARL, DANIEL A.	
	Examiner	Art Unit	
	Tracy Dove	1745	

-- ***The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/22/04*.

2. ☒ The allowed claim(s) is/are *42-76*.

3. ☒ The drawings filed on *31 October 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/31/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *attached* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Julia Dierker on 12/7/04.

The application has been amended as follows:

In the specification:

At page 1, after line 10, replace the present paragraph with:

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional of application S.N. 09/839,956, filed April 19, 2001, now U.S. Patent 6,677,070.

In the claims:

1 – 41 (Cancel)

42. (Currently amended) A method of making a fuel cell, the method comprising the steps of:

creating a well in a dielectric or semiconductor substrate, the substrate having a first side and a second side, the second side opposed to the first side, and the well being defined in the first side;

depositing a thin film solid oxide electrolyte layer on ~~the~~ a surface of the well;

applying an electrode layer in the electrolyte coated well;

creating a counter well in the second side, the counter well abutting the electrolyte layer; and

applying a counter electrode layer in the counter well.

43. (Currently amended) The method as defined in claim 42 wherein the step of depositing the electrolyte layer is performed by at least one of sputter deposition ~~and~~ or chemical vapor deposition (CVD).

44. (Original) The method as defined in claim 42, further comprising the step of firing the electrolyte layer prior to application of the electrode layer.

45. (Original) The method as defined in claim 42, further comprising the step of applying an isolation dielectric on the second side of the substrate.

46. (Currently amended) The method as defined in claim ~~42~~ 45 wherein the substrate is silicon, and wherein the isolation dielectric is grown on the second side of the substrate.

47. (Original) The method as defined in claim 42, further comprising the step of processing the electrode layer and the counter electrode layer using planarization techniques.

48. (Currently amended) The method as defined in claim ~~42~~ 47 wherein the planarization is performed by at least one of chemical mechanical polishing (CMP) ~~and~~ or mechanical polishing.

49. (Original) The method as defined in claim 42, further comprising the step of applying a hard mask to the first side of the substrate before the step of creating a well.

50. (Original) The method as defined in claim 49 wherein the substrate is silicon, and wherein the first side hard mask is grown on the substrate first side.

51. (Original) The method as defined in claim 42, further comprising the step of applying a hard mask to the second side of the substrate before the step of creating a counter well.

52. (Original) The method as defined in claim 51 wherein the substrate is silicon, and wherein the second side hard mask is grown on the substrate second side.

53. (Original) The method as defined in claim 42 wherein the step of creating the well and the step of creating the counter well are each carried out by etching.

54. (Currently amended) The method as defined in claim ~~42~~ 53 wherein the substrate is silicon, and wherein the etching is performed by an etchant selected from the group consisting of wet anisotropic etchants, plasma anisotropic etchants, and mixtures thereof, thereby forming ultra-smooth surfaces on the well and the counter well.

55. (Original) The method as defined in claim 54 wherein the wet anisotropic etchants are selected from the group consisting of potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), a mixture of potassium hydroxide and isopropyl alcohol, ammonium hydroxide, sodium hydroxide, cerium hydroxide, ethylene diamine pyrocatechol, and mixtures thereof.

56. (Original) The method as defined in claim 54 wherein the plasma anisotropic etchant is sulfur hexafluoride alternated with C_4F_8.

57. (Currently amended) The method as defined in claim ~~42~~ 53 wherein the substrate is a silicon oxide containing dielectric substrate, and wherein the etching is performed by a hydrofluoric containing isotropic etchant.

58. (Currently amended) The method as defined in claim 42 wherein the substrate is selected from the group consisting of single crystalline silicon, polycrystalline silicon, silicon oxide containing dielectric ~~substrates~~ substrate, alumina, sapphire, ceramic, and mixtures thereof.

59. (Original) The method as defined in claim 58 wherein the substrate is single crystalline silicon.

60. (Currently amended) The method as defined in claim 42 wherein at least one of the ~~well and the counter well is adapted to contain~~ electrode layer contained in the well or counter electrode layer contained in the counter well is a thick film electrode layer.

61. (Currently amended) The method as defined in claim 60 wherein the electrode layer contained in the well ~~contains~~ is a thick film electrode layer and the counter electrode layer contained in the counter well ~~contains~~ is a thick film counter electrode layer.

62. (Currently amended) A method of making a fuel cell, the method comprising the steps of:

creating a well in a dielectric or semiconductor substrate, the substrate having a first side and a second side, the second side opposed to the first side, and the well being defined in the first side;

depositing a thin film solid oxide electrolyte layer on ~~the~~ a surface of the well, wherein the step of depositing the electrolyte layer is performed by at least one of sputter deposition ~~and~~ or chemical vapor deposition (CVD);

applying an electrode layer in the electrolyte coated well;

creating a counter well in the second side, the counter well abutting the electrolyte layer, wherein the step of creating the well and the step of creating the counter well are each carried out by etching;

applying an isolation dielectric on the second side of the substrate;

applying a counter electrode layer in the counter well; and

processing the electrode layer and the counter electrode layer using planarization techniques, wherein the planarization is performed by at least one of chemical mechanical polishing (CMP) ~~and~~ or mechanical polishing.

63. (Original) The method as defined in claim 62, further comprising the step of firing the electrolyte layer prior to application of the electrode layer.

64. (Original) The method as defined in claim 62 wherein the substrate is silicon, and wherein the isolation dielectric is grown on the second side of the substrate.

65. (Original) The method as defined in claim 62, further comprising the step of applying a hard mask to the first side of the substrate before the step of creating a well.

66. (Original) The method as defined in claim 65 wherein the substrate is silicon, and wherein the first side hard mask is grown on the substrate first side.

67. (Original) The method as defined in claim 62, further comprising the step of applying a hard mask to the second side of the substrate before the step of creating a counter well.

68. (Original) The method as defined in claim 67 wherein the substrate is silicon, and wherein the second side hard mask is grown on the substrate second side.

69. (Original) The method as defined in claim 62 wherein the substrate is silicon, and wherein the etching is performed by an etchant selected from the group consisting of wet anisotropic etchants, plasma anisotropic etchants, and mixtures thereof, thereby forming ultra-smooth surfaces on the well and the counter well.

70. (Original) The method as defined in claim 69 wherein the wet anisotropic etchants are selected from the group consisting of potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), a mixture of potassium hydroxide and isopropyl alcohol, ammonium hydroxide, sodium hydroxide, cerium hydroxide, ethylene diamine pyrocatechol, and mixtures thereof.

71. (Original) The method as defined in claim 69 wherein the plasma anisotropic etchant is sulfur hexafluoride alternated with C_4F_8.

72. (Original) The method as defined in claim 62 wherein the substrate is a silicon oxide containing dielectric substrate, and wherein the etching is performed by a hydrofluoric containing isotropic etchant.

73. (Currently amended) The method as defined in claim 62 wherein the substrate is selected from the group consisting of single crystalline silicon, polycrystalline silicon, silicon oxide containing dielectric ~~substrates~~ substrate, alumina, sapphire, ceramic, and mixtures thereof.

74. (Original) The method as defined in claim 73 wherein the substrate is single crystalline silicon.

75. (Currently amended) The method as defined in claim 62 wherein at least one of the ~~well and the counter well is adapted to contain~~ electrode layer contained in the well or counter electrode layer contained in the counter well is a thick film electrode layer.

76. (Currently amended) The method as defined in claim 75 wherein the electrode layer contained in the well ~~contains~~ is a thick film electrode layer and the counter electrode layer contained in the counter well ~~contains~~ is a thick film counter electrode layer.

77-80. (Canceled)

Allowable Subject Matter

Note the above Examiner amendments were required to correct formal matters (35 U.S.C. 112, 2nd issues) only and were not made to overcome the prior art of record.

Claims 42-76 are allowed.

The following is an examiner's statement of reasons for allowance: the claims are directed toward a method of making a fuel cell wherein the method comprises the steps of creating a dielectric or semiconductor substrate having a well defined in a first side of the substrate. An electrolyte is deposited on a surface of the well and an electrode layer is applied in the electrolyte coated well. A counter well is created in a second side of the substrate and abuts the electrolyte layer. A counter electrode layer is applied in the counter well. The electrolyte between the electrode layer and the counter electrode layer is contained within the substrate. Both electrodes and the electrolyte are contained within a single substrate.

The prior art does not teach the claimed invention. Ohlsen et al. (US6,641,948) teaches fuel cells having silicon substrates and/or sol-gel derived support structures. However, the anode is contained in a first silicon substrate and the cathode is contained in a second silicon substrate. Ohlsen does not teach the anode and cathode are contained within the same silicon substrate. Furthermore, an electrolyte layer (704) is not contained within the silicon substrate, as required by the claimed invention.

Marsh (US6,312,846) teaches a fuel cell that is formed on a semiconductor wafer by etching a channel in the wafer and forming a proton exchange membrane (PEM) barrier in the

etched channel. Marsh does not teach the anode and cathode are contained within the semiconductor water. The claimed invention requires a well formed in a first surface of the substrate and a counter well formed in a second surface of the substrate. Marsh teaches a single channel is etched in a single surface of the semiconductor wafer. Marsh teaches the fuel cell is formed on the wafer, not within the wafer. Marsh does not teach an electrode layer applied in a well and a counter electrode layer applied in a counter well wherein the electrode layer abuts a first surface of the electrolyte contained within the substrate and a counter electrode layer abuts a second surface of the electrolyte layer contained within the substrate.

Kearl (US6,677,070) teaches the claimed invention (see at least Figs. 13 and 15), however, Kearl is not available as prior art against the claimed invention. The present application is a divisional application of Kearl (US6,677,070). There is no double patenting between the Kearl patent and the claimed invention because the claims of the Kearl patent do not contain the limitation of creating a well and a counter well in a dielectric or semiconductor substrate. Furthermore, the claimed invention does not require an electrolyte consisting essentially of Ta_2O_5, as required by the Kearl patent.

Kearl (US2004/0101729) teaches the claimed invention (see at least Figs. 13 and 15), however, Kearl is not available as prior art against the claimed invention. Kearl (US2004/0101729) is a continuation of Kearl (US6,677,070). Note the present application was filed in response to a restriction requirement, mailed 4/20/04, required by Examiner Winter in application 10/680,778 (US2004/0101729).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Malhi (US5,789,093) teaches a fuel cell comprising a ceramic or graphite material manifold.

Lehmann et al. (US5,262,021) teaches a method of manufacturing a perforated semiconductor workpiece.

George et al. (US6,361,893) teaches a planar fuel cell utilizing nail current collectors for increased active surface area.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tracy Dove whose telephone number is 571-272-1285. The examiner can normally be reached on Monday-Thursday (9:00-7:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pat Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tracy Dove
Patent Examiner
Technology Center 1700
Art Unit 1745

December 3, 2004